1. An integrated circuit, comprising:

a random access memory (RAM) storage located on a semiconductor chip; and

a controller located on the semiconductor chip and coupled to read data from and write data to the RAM storage, the controller being programmable to perform bitwise operations on data words stored in the RAM.

2. The integrated circuit of claim 1, wherein the controller can perform a bitwise operation in response to receiving a mask word, the form of the operation being defined by the mask word.

3. The integrated circuit of claim 2, wherein the controller is configured to operate on bits of the data word that correspond to bits of the mask word having a preselected value.

4. The integrated circuit of claim 3, wherein the controller is configured to perform one of bitwise set and a bitwise clear.

5. The integrated circuit of claim 2, wherein the controller is configured to perform one of bitwise ``test and set'' and bitwise ``test and clear''.

6. The integrated circuit of claim 2, wherein the controller is configured to perform an increment operation on the data words.

7. The integrated circuit of claim 2, further comprising:

a plurality of processing engines located on the integrated chip and coupled to program the controller.

8. The integrated circuit of claim 7, wherein the controller is coupled to receive data from and write data to the processing engines.

9. The integrated circuit of claim 8, wherein the controller is coupled to receive a mask word from one of the processing engines in response to the one of the processing engines programming the controller.

10. A method of operating on data, comprising:

receiving a command for bitwise operation at a pull engine;

retrieving a mask word from an engine that sent the command;

sending the mask word and a request for the command from the pull engine to a controller; and

performing a bitwise operation on a data word stored in a RAM storage in response to the request, the mask word

defining the location of one or more bits of the data word on which the operation is performed.

11. The method of claim 10, wherein the performing operates on bits of the data word that correspond to bits of the mask word with a preselected value.

12. The method of claim 11, wherein the performing includes doing one of a bitwise set and a bitwise clear on the data word.

13. The method of claim 10, further comprising:

sending a copy of the data word to the engine.

14. The method of claim 10, wherein the command selects the data word from among more than 500 data words stored in the RAM storage.

15. A network processor, comprising:

a parallel set of engines for processing data packets;

a bus interface to transmit and receive the data packets; and

a shared scratchpad memory coupled to receive commands from the engines, the scratchpad memory providing RAM storage for the engines, and capable of performing bitwise operations on data words stored therein in response

to commands and mask words received from the engines, the mask words defining bits affected by the operations.

16. The network processor of claim 15, wherein the engines and the bus interface are located in one integrated circuit.

17. The network processor of claim 15, further comprising:

a RAM coupled to the engines and to the bus interface, the engines capable of writing received data packets from the bus interface to the RAM and of sending data packets from the RAM to the bus interface.

18. The network processor of claim 17, further comprising:

a bus coupled to the bus interface; and

a plurality of devices connected to the bus, each of the devices to transmit data packets between an associated network and the bus.

19. The network processor of claim 18, wherein the bitwise operations include one of a set operation and a clear operation.

20. A computer program product for processing data packets that resides on a machine readable medium and comprises instructions for causing a processing engine to:

send a command to a pull engine, the command requesting a bitwise operation be performed on a data word stored in a scratchpad memory; and

write a mask word for the operation to an output transfer register readable by the engine, the mask word defining the location of one or more bits of the data word on which the operation is performed.

21. The computer program product of claim 20, wherein bits of the mask word having a preselected value define bits of the data word upon which the bitwise operation operates.

22. The computer program product of claim 20, wherein the command requests one of a bitwise set and a bitwise clear on the data word.

23. The computer program product of claim 20, the instructions further cause the processing engine to:

read a copy of the data word sent from the scratchpad to the engine.